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ENIAC'owe Spectrum

Upgrade described in Informik III/1987, in article "Jak z ZX SPECTRUM zrobić komputer. Zmieniamy architekturę komputera." ("How to make a computer from ZX SPECTRUM. We change architecture of computer.") by Wojciech Apel.

The upgrade is very interesting. Especially because it was designed in year 1985, the same time when **ZX Spectrum 128K**.

A latch was added as a port at 62 (#3E) address (ULA is disabled for A7=0 and A6=0). Ouputs of this latch are called **S0**, **S1**, **S2**, **S3**, **S4** (in tables shown also as binary values range %00000..%11111). Also there are two extra switches to select confuguration. First of them is called **TRYB** and selects between ZX and CP/M modes. Second switch is called **BANK** and selects 32kB bank. As a result there are several possible configurations...

Memory map after upgrade

Table 1. Switch **TRYB** set to ZX.

Section	Memory bank			
D **(#C000..#FFFF)**			URAM3 S4=1 & BANK=1	URAM1 S4=0 | BANK=0
C **(#8000..#BFFF)**			URAM2 S4=1 & BANK=1	URAM0 S4=0 | BANK=0
B **(#4000..#7FFF)**			VRAM	
A **(#0000..#3FFF)**	EPROM S0=0		ROM S0=1	

Table 2. Switch TRYB set to CP/M.

Section	Memory bank			
D **(#C000..#FFFF)**		URAM3		
C **(#8000..#BFFF)**		URAM2		
B **(#4000..#7FFF)**		VRAM S2=0 %xx0xx	URAM1 S2=1 %xx1xx	
A **(#0000..#3FFF)**	EPROM S0=0 %xxxx0	ROM S0=1 & S1=0 %xxx01	URAM0 S0=1 & S1=1 & S3=0 %x0x11	URAM0* S0=1 & S1=1 & S3=1 %x1x11

URAM0, URAM1, URAM2, URAM3 - 4 × 16kB "upper" RAM banks
VRAM - 16kB "lower" RAM with screen
ROM - original ROM
EPROM - 4kB or 8kB boot EPROM
URAM0* - with write protection

Similar upgrade

Please have a look for a link to alternative ROMs balow and the **80-LEC.ROM** there. It has support for 32kB bank in lower half of memory, switched by bit 0 of #FD port. Data can be copied with `MOVE` command and strange syntax.

Missed idea

It is incredible, how easy could the **ZX Spectrum 48K** be upgraded to get 64kB RAM all RAM mode! (The ROM and video RAM are in separate bank.) It was enough to replace 32kB RAM with 64kB chips and connect A15 to multiplexer input (in place of jumper). But A15 line must be separated with 680ohm resistor - the ULA A15 input and the top memory logic circuit must be behind it.

Then we add 74LS74, of which we need only one latch is needed. The /R input should be connected to /RESET line, D input to one of lines D5..D7 and /CLK to /WR ORed /IORQGE ORed (with 680ohm resistor and diode). So the latch (1bit register) expands the 254 port used by ULA. When 0 is written, the normal 16kB ROM + 48kB RAM architecture is used. But when 1 is written to latch, its non-inverted output forces (with diode) high state on the part of A15 line sepated by resistor. So there's no access to ROM and VRAM, while "upper" memoy decoder activates RAM for all 64kB of address space.

Needed parts: eigth 4164 chips, one 74LS74, two 680ohm resistors, two 1N4148 diodes and some wires. Perhaps a switch to lock this feature for better compatibility with some strange written software, that uses `IN A,(#FE): OUT (#FE),A`...

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